**Logic Interface Board PCB Test Log**

HW part number: HW002

HW revision: R001

Firmware version: N/A

Software version: N/A

Test case: board bring up

Test date: 2018-07-04

|  |  |
| --- | --- |
| **Test power supplies**  Apply +5V to 5V power rail.  Verify 5.0V appears at 5.0V power rail.  Verify 3.3V appears at 3.3V power rail. | Pass  Pass |
| **Investigative notes (mode LED still not working)**  Power up sequence  0 – 5.0 V in 2.5 usec  May not be a problem, will have to see what the microcontroller and FPGA ramp times are, and if there are problems with them.  PIC24FJ128GB204 datasheet calls out 0-3.3V in 66 ms. | **Design** |

Summary

Potential design flaw in power supply circuitry: ramp rates may be too fast.

HW part number: HW002

HW revision: R002

Firmware version: initial, unreleased test firmware

Software version: N/A

Test case: board bringup

Test date: 2018-05-13

|  |  |
| --- | --- |
| **Test mode LED**  Apply +5V to 5V power rail.  Verify 1.2V appears at 1.2V power rail.  Verify 3.3V appears at 3.3V power rail.  Initiate debug session  Verify ICSP connection succeeds  Verify TRIS direction register sets RB4 (mode LED, pin33) to output  Verify LATB register sets RB4 output (mode LED, pin33) to low level (0.0 - 0.7 V)  Verify Mode LED illuminates | Pass  Pass  Pass  Pass  Pass  Pass |

Summary

RB4 (MODE, pin 33) and RA4 (CRESET, pin 34) are listed as input only in the device datasheet.

Bridging pins 32 and 33, and changing MODE logic (software) from RB4 (pin 33) to RA8 (pin 32) corrects the problem.

The FPGA reports as being configured correctly. Since the device presumably cannot assert CRESET, I assume this is because the FPGA simply waits for its configuration image until the MCU provides it.